IN THE CLAIMS

1 (Currently Amended). A method comprising:

forming a phase change memory including a phase change storage element and a phase change threshold switch; ~~and~~

forming the storage element and the threshold switch within a memory area and providing a periphery beside said memory area, said periphery including no memory elements; and

forming a damascene via to a conductive line in said ~~the~~ periphery ~~of said phase change memory~~.

Claim 2 (Canceled).

3 (Previously Presented). The method of claim 1 including forming said switch over said element.

4 (Previously Presented). The method of claim 3 including forming, in said memory, a pore over a substrate, said pore having a dimension smaller than the feature size possible with lithographic techniques.

5 (Original). The method of claim 4 including forming said pore by forming an aperture through an insulator and forming a sidewall spacer in said aperture.

6 (Previously Presented). The method of claim 5 including forming a lower electrode of said phase change storage element in said pore.

7 (Previously Presented). The method of claim 1 including forming a barrier layer between said threshold switch and said storage element.

8 (Previously Presented). The method of claim 1 including forming an upper electrode over said phase change storage element, said upper electrode having a vertical extent at least twice its horizontal extent.

9 (Currently Amended). The method of claim 1 including forming an electrode over said phase change storage element ~~and said threshold switch~~, said electrode having sidewall spacers.

10 (Original). The method of claim 9 including using said sidewall spacers as a mask to etch through underlying layers.

11 (Previously Presented). The method of claim 1 wherein forming said phase change memory includes forming a memory array including a plurality of memory cells as a plurality of integrated islands spaced from one another.

12 (Original). The method of claim 11 including filling the regions surrounding said islands with an insulator.

13 (Previously Presented). The method of claim 12 including forming said insulator to a height over the upper extent of said islands.

14 (Previously Presented). The method of claim 13 including forming grooves through said insulator down to and past the upper extent of said islands.

15 (Currently Amended). The method of claim 13 including forming a vertical groove in said memory array and a vertical groove in a periphery <u>beside said memory array</u>.

16 (Original). The method of claim 15 including filling said groove in said periphery with a sacrificial light absorbing material.

17 (Currently Amended). The method of claim 16 including etching said ~~groove in said periphery into said~~ sacrificial light absorbing material in said groove in said periphery.

18 (Previously Presented). The method of claim 17 wherein forming a damascene via includes filling said groove in the periphery with a conductive material.

19 (Previously Presented). The method of claim 18 including forming said groove in said periphery deeper than said groove in the memory array.

20 (Previously Presented). The method of claim 19 including forming said groove in said periphery to a depth below the upper extent of said upper electrode and above the lower extent of said upper electrode.

21 (Previously Presented). An apparatus comprising:

a phase change memory including a phase change storage element and a phase change threshold switch;

a conductive line coupled to said phase change storage element and said phase change threshold switch; and

a via to said conductive line.

Claim 22 (Canceled).

23 (Previously Presented). The apparatus of claim 21 wherein said switch is formed over said element.

24 (Previously Presented). The apparatus of claim 23 wherein said memory includes a substrate, a pore over said substrate, said pore having a dimension smaller than the feature size possible with lithographic techniques.

Claim 25 (Canceled).

26 (Previously Presented). The apparatus of claim 24 including an electrode for said phase change storage element in said pore.

27 (Previously Presented). The apparatus of claim 21 including a barrier layer between said threshold switch and said storage element.

28 (Previously Presented). The apparatus of claim 21 including an upper electrode having a vertical extent at least twice its horizontal extent, said upper electrode formed over the phase change storage element.

29 (Previously Presented). The apparatus of claim 21 wherein said memory includes an insulator and said via includes a metal line extending through said insulator.

Claims 30-36 (Canceled).